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| 10/056,426 | 01/23/2002 | Naoyuki Kawabe | 2102487-991160 | 8080 |

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| EXAMINER | |
|---|---|
| LIN, SUN J | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2825 | |

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/056,426 | KAWABE ET AL. | |
| | Examiner | Art Unit | |
| | Sun J Lin | 2825 | |

*-- The MAILING DATE of this communication appears on the cover she t with the correspond nce address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *23 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01/23/2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/23/02, 07/22/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This office action is in response to application 10/056,426 filed on 01/23/2002.

Claims 1 – 12 remain pending in the application.

### *Drawing Objections*

2. Drawings are objected to because of following informalities:

Fig. 1 should be labeled as a —(PRIOR ART)—.
Fig. 1 should include labels P1 and P2 as indicated on page 2, line 17.
Fig. 2 should be labeled as a —(PRIOR ART)—.
Fig. 5 should be labeled as a —(PRIOR ART)—.
Fig. 6 should be labeled as a —(PRIOR ART)—.

Appropriate correction is required.

### *Claim Objections*

3. Claims listed below are objected to because of the following informalities:

Claim 1, line 3, change "analyzing" to —analyze—.
Claim 1, line 10 – 11, delete —calculating the leakage currents of the circuit,—.
Claim 2, line 9 – 10, delete —calculating the leakage currents of the circuit,—.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

(1). Determining the scope and contents of the prior art.
(2). Ascertaining the differences between the prior art and the claims at issue.
(3). Resolving the level of ordinary skill in the pertinent art.
(4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1 – 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,687,883 B2 to *Cohn et al.* in view of IEEE Paper titled " *Stand-by Power Minimization through Simultaneous Threshold Voltage Selection and Circuit Sizing*" to *Sirichotiyakul et al.*

6. As to Claims 1 and 2, *Cohn et al.* show and disclose the following subject matter:

- *System* and *method* for inserting *leakage reduction control* in logic circuits – [title; Fig. 6]; Notice that Fig. 6 shows an automatic circuit generation method/system for inserting *leakage reduction control*;
- Receiving *netlist 202* (i.e., *circuit generation information*) from input – [Fig. 6]; Notice that the *netlist* includes sufficient information for use in generating *circuit connection data* for a *logic circuit* under study;
- IEEE Paper titled " *Stand-by Power Minimization through Simultaneous Threshold Voltage Selection and Circuit Sizing*" to *Sirichotiyakul et al.* on minimization of leakage – [col. 2, line 1 – 9].

*Cohn et al.* teach receiving a *netlist* (*circuit generation information*), which contains sufficient information for use in generating *circuit connection data* for a *logic circuit* under study, they do not teach using the net list to generate leakage current data for the logic circuit. But *Sirichotiyakul et al.* show in Fig. 2 a *circuit schematic* (i.e., *netlist*) of a 3-input NAND gate and a table listing *leakage current data* for all *possible states* of signals at *input nodes ABC*. Notice that the *leakage current data* provides a design engineer useful information in specifying appropriate signal states at input nodes of the 3-input NAND gate in order to minimize leakage current consumption during stand-by mode.

Therefore, it whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Sirichotiyakul et al.* in generating *leakage current data* associated with circuit schematic of a *logic circuit* under

study in order to provide useful information in specifying appropriate signal states at input nodes of the logic circuit to minimize leakage current consumption during its stand-by mode.

In addition to reasons listed above, *Cohn et al.* and *Sirichotiyakul et al.* teach the following subject matter:

- *Test vectors* for generating *state vectors* as input signals to be fed at *input node* of a 3-input NAND gate, which has three (3) input pins ABC – [*Sirichotiyakul et al.*; Fig. 2]; As indicated in Fig. 2, the input node has eight (8) states; Notice that the *test vectors* are received for operating the 3-input NAND gate;
- *Input state probabilities* – [*Sirichotiyakul et al.*; page 437, right col. line 8 – 9];
- Setting of *logic state of signals* in order to minimize leakage – [*Cohn et al.*; col. 2, line 11 – 12]; A set of logic values (i.e., *state vector*) at input pins that causes "*low leakage state*" may be called "low leakage *vector*" – [*Cohn et al.*; col. 1, line 39 – 41]; Probabilities of various input states – [col. 2, line 64]; Notice that each state has different probability;
- Provide a *logic system design methodology* that *forces the states of logic gates (to change by any means)* based on *probabilistic analysis* in order to *reduce the leakage* – [*Cohn et al.*; col. 2, line 33 – 52]; Notice that this *logic system design methodology* include *switching input signals between exchangeable pins* without affecting logic function;
- Estimated minimum *leakage current* of a *logic gate* by summing over *leakage under combination of input values* (i.e., exchanged state vectors) multiplied by *probability of occurrence* of that combination of input values – [*Cohn et al.*; col. 3, line 7 – 11]; Notice that a logic circuit may contain a plurality of logic gates, therefore, a plurality leakage currents need to be computed in order to estimate the overall leakage current; State vectors are varying due to pin assignment change;
- Exit and output updated netlist of the logic circuit – [*Cohn et al.*; Fig. 6]; Notice that, at "EXIT", the netlist received at 202 is updated to include all pin assignment changes.

For reference purposes, the explanations given above in response to Claims 1 and 2 are called **[Response A]** hereinafter.

7. As to Claim 3, reasons are included in **[Response A]** given above. Notice that all explanations included in **[Response A]** on an automatic circuit generation method can be applied in development of a computer embodied on a computer-readable medium for generating circuits.

8. Claims 4 – 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,687,883 B2 to *Cohn et al.* and IEEE Paper titled " *Stand-by Power Minimization through Simultaneous Threshold Voltage Selection and Circuit Sizing*" to *Sirichotiyakul et al.* in view of U.S. Patent No. 6,212,655 B1 to *Zarkesh et al.*

9. As to Claim 4, *Cohn et al.* and *Sirichotiyakul et al.* teach an automatic circuit generation system for generating a *logic circuit* through performing *node state (i.e., state vector) analyzing*, *leakage current estimating* and *outputting updated netlist (i.e., circuit information)* on a logic circuit as recited in **[Response A]** given above. Notice that the logic circuit under study is a object circuit, which is composed of a plurality of logic cells. *Cohn et al.* and *Sirichotiyakul et al.* do not teach generating the logic circuit (object circuit) by use of cell library including logic cells. But *Zarkesh et al.* teach *efficient power analysis method* for electronic circuit design of *logic cells* with many output switches – [title; abstract]. *Zarkesh et al.* also teach the following subject matter:

- *Cell library* having a *power model* corresponding to a *cell instance* – [abstract]; *Cell library* includes a *power model library 112* – [Fig. 3A]; Notice that a *cell instance* is a *logic cell*, and *power model library* contains a plurality power models. Therefore *cell library* include *power models* for a plurality of logic cells;
- *Leakage current* tends to increase for *low threshold (logic) device* – [col. 3, line 53 – 54].

Notice that, based on reasons listed above, *Zarkesh et al.* teach storing *power models* of a plurality of *logic cells* in a *cell library* in order to provide a design engineer a useful reference in designing a low leakage logic circuit by using logic cells included in the cell library.

Therefore, it whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Zarkesh et al.* in storing *power models* of a plurality of *logic cells* in a *cell library* in order to provide a design engineer a useful reference in designing a low leakage logic circuit by using logic cells included in the cell library.

For reference purposes, the explanations given above in response to Claim 4 are called **[Response B]** hereinafter.

10. As to Claim 9, reasons are included in **[Response B]** given above. Notice that all explanations included in **[Response B]** on *an automatic circuit generation method for generating an object circuit by use of a cell library including logic cells* can be applied in development of a computer embodied on a computer-readable medium for generating circuits.

11. As to Claims 5 and 10, in addition to reasons included in **[Response B]** given above, *Cohn et al.* teach proving a logic system design methodology for minimizing leakage current passing through the object circuit when the object current is in activated in a standby state – [col. 2, line 33 – 52].

12. As to Claim 6, in addition to reasons included in **[Response B]** given above, *Cohn et al.* teach proving a logic system design methodology for minimizing leakage current passing through the object circuit when the object current is activated and operating in a normal state – [col. 2, line 33 – 52].

13. As to Claims 7 and 11, reasons are included in **[Response A]** and **[Response B]** given above. Notice that *Zarkesh et al.* storing *(low leakage) power models* in *cell library* for use as reference for the low leakage circuit design and patterns of the object circuit (low leakage logic circuit).

14. As to Claims 8 and 12, *Cohn et al.* teach that, based on probability and switching analysis, (leakage current) results are measured – [col. 14, line 16 – 32].

***Conclusion***

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J. Lin whose telephone number is (571) 272-1899. The examiner can normally be reached on Monday-Friday (9:00AM-6:00PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Sun James Lin
Art Unit 2825
July 9, 2004